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THE ARITHMETIC UNIT OF DACICC—200 COMPUTER

by

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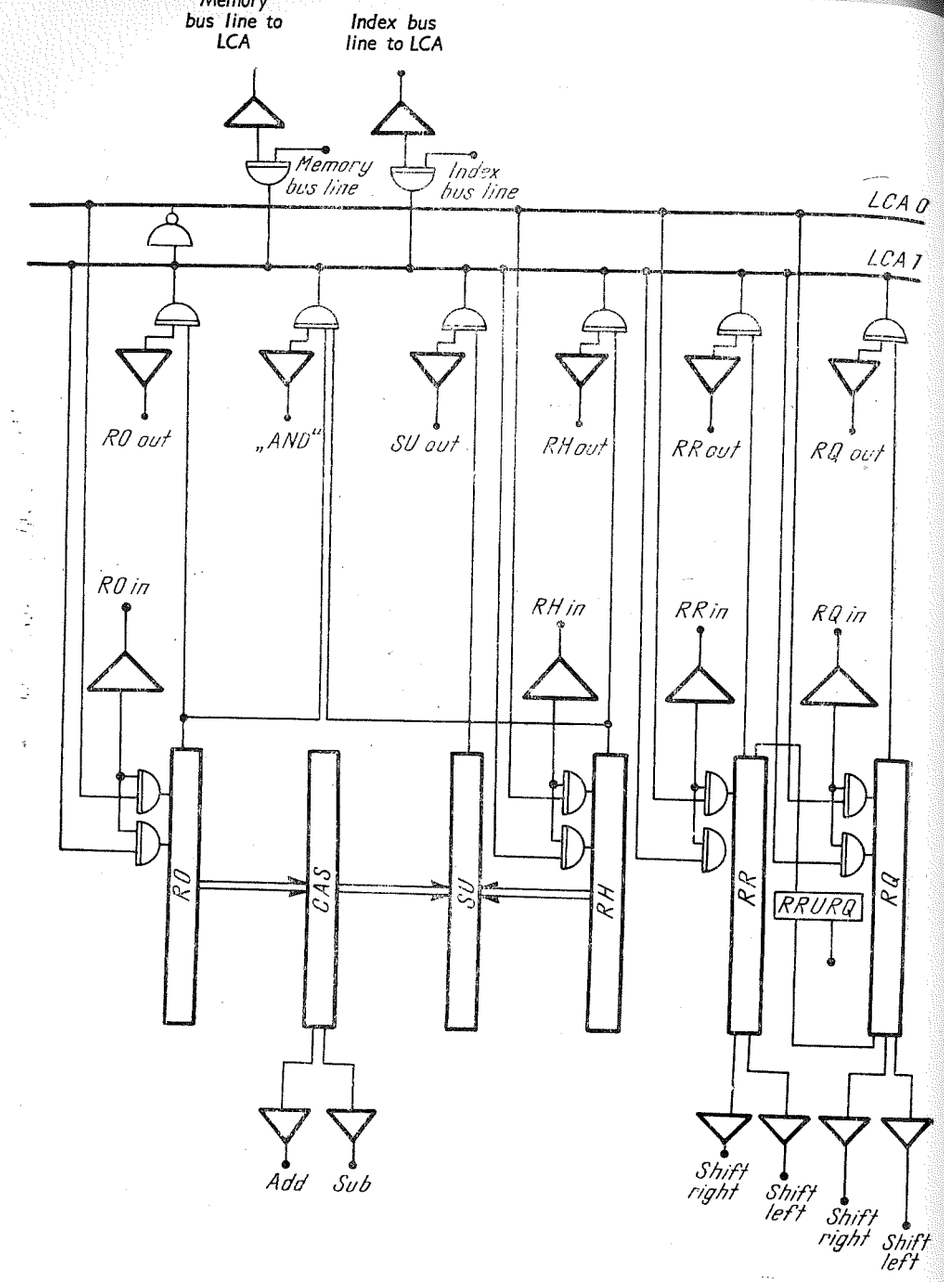
The purpose of the present paper is to show the logic design and some practical solutions of the DACICC-200's parallel arithmetic unit. We will lay out briefly the circuit problems, the binary adder and carry propagation circuits, and the configuration of registers, but without the control unit to supervise arithmetic operations in fixed and floating point, these operations being effected by the central control unit.

To begin with, the basic circuitry element is a standardised one for the whole computer : double level diode gate logic followed by an inverting amplifier (The semiconductor elements are : EFD-115 diode and EFT-319 transistor). The fan-in / fan-out capacity is 4 to 6, with 30 ns delay over an element. The pilot-frequency of computer is 2 Mcycles.

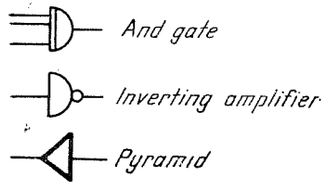
The main part of arithmetic unit, the synchronous parallel adder is not accumulative. It has 49 orders of which 39 represent the sign and mantissa, and 10 orders form the exponent. The sum and carry are produced using eight diode gates and two inverting amplifiers. Due to the property of inverting the output logic in accordance with input logic in standardised electronic circuits, it is convenient that the orders of adder stages be not uniform — consequenthy they present an alternate logic. Note that in this way an improvement in speed, eliminating a circuit delay per order and economical advantages are obtained as compared with many other adder solutions.

The central problem in the design of the high-speed arithmetic unit was the minimisation of the time which had to be allowed for the possible worst-case propagation of carry by the adder elements, because it had a decisive influence upon the time of execution of arithmetic operations. Among various solutions that were analysed, the carry-skip method [1] by which a good compromise between speed and hardware expenditure is achieved, was chosen.

The reduction of the maximum carry propagation time depends on the number and distribution of carry skips. However, the structure of this adder (alternate logic) imposes additional conditions to carry skip distributions. In particular, the skips may comprise only odd num-



Symbols



bers of adder positions and their distribution relative to one another is always an even number of positions. In this assumption the carry-skip circuit operates in maximum 11 time units (the worst-case experimentally measured is of 270 ns) over the mantissa. It has thirteen subgroups, of 3-bit stages each, further combined into three groups of equal sizes.

Let us examine the block diagram of arithmetic unit (fig. 1). The bus line (LCA) realises the communication between the adder, registers and the other parts of the computer. There is an operating register (RO), which holds either the augend or subtrahend and enters these numbers in adder (SU) via addition / subtraction switch (CAS). This switch forms the converse of the number if it is needed. The helping register (RH) holds either the addend or minuend and it is fed permanently to the adder. The result register (RR) holds the result of the arithmetic operation; it forms an unitary register with product-quotient register (RQ) when it multiplies or divides and in some shifting operations. It is provided to execute logical operations by hardware in arithmetic unit.

In order to handle the parallel inputs and outputs of the arithmetic units, pyramids of amplifiers for control signals are built in.

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BIBLIOGRAPHY

1. M. Lehman and N. Burla: *Skip Technique for High-Speed Carry-propagation in Binary Arithmetic Units*, IRE TRANS. on Electronic Computers, Number 4, 1961
2. S. Majerski: *On Determination of Optimal Distributions of Carry Skips in Adders*, IEEE TRANS. on Electronic Computers, Number 1, 1967.
3. J. Sklansky and M. Lehman: *Ultimate-Speed Adders*, IEEE TRANS. on Electronic Computers, Number 2, 1963.
4. R. K. Richards: *Arithmetic Operations in Digital Computers*, 1955.